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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GUY L. STEELE, JR

Appeal 2008-005881
Application 10/035,580
Technology Center 2100

Decided: May 27, 2010

Before HOWARD B. BLANKENSHIP, ST. JOHN COURTENAY III, and THU A. DANG, *Administrative Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-40, which are all the claims in the application. We have jurisdiction under 35 U.S.C. § 6(b).[1]

We affirm, but designate our decision as a new ground of rejection.

Invention

Appellant's invention relates to systems and methods for performing floating point multiplication with embedded status information associated with a floating point operand. Spec. ¶ [002].

Representative Claim

1. A system for providing a floating point product, comprising:

an analyzer circuit configured to determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively; and

a results circuit coupled to the analyzer circuit and configured to assert a resulting floating point operand containing the product of the first floating point operand and the second floating point operand and a resulting status embedded within the resulting floating point operand.

[1] This appeal relates to several earlier appeals, listed at page 3 of the Appeal Brief.

Examiner's Rejection

Claims 1-40 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Huang (US 5,995,991).

In the Final Rejection, the Examiner applied a provisional rejection under the judicially created doctrine of obviousness-type double patenting. Appellants indicate (App. Br. 7 n.1) that they do not request review of the double patenting rejection. In any event, the Examiner did not repeat the provisional rejection in the Answer, which indicates that the rejection has been withdrawn. *See Ex parte Emm*, 118 USPQ 180, 181 (Bd. App. 1957) (rejection not referred to in the examiner's answer is assumed to have been withdrawn). We conclude that the provisional rejection for obviousness-type double patenting is not before us.

FINDINGS OF FACT

Huang

1. Huang discloses that "[i]f the generation of the result produces one of a predetermined set of special operands, a tag generator also generates a tag having a predetermined tag value corresponding to the produced special operand. Col. 5, ll. 43-46.

2. "[E]ach of the registers 116 and 118 has an operand value storage portion 116-1 and 118-1 and a tag value storage portion 116-2 and 118-2." Col. 6, l. 66 - col. 7, l. 2.

3. Figures 1-3 of Huang show a conventional arithmetic calculation circuit where one or more operands x and y are supplied from a memory device such as a register file 12. The operands x and y are inputted to an arithmetic section 14. Col. 1, ll. 40-42.

4. In the conventional circuit, a zero value result (+ or -) is represented by an operand where (col. 1, ll. 56-64):

sign='0' or '1' bit,

exponent=a sequence of eight '0' bits,

magnitude=a sequence of twenty-three '0' bits.

5. In the conventional circuit, when the arithmetic section 14 performs an operation that results in a value other than an ordinary operand value, the arithmetic unit outputs a signal indicating that the result is zero, infinity or not a number to the generator circuit 22. In response, the circuit 22 generates the appropriate output floating point number as per the IEEE standard of special operands set. Col. 2, ll. 55-59.

6. In the conventional circuit, interposed between the register file and the arithmetic section 14 are detectors 24 and 26. One detector 24 or 26 is provided for each operand input path. The detectors 24 and 26 each receive a respective operand x or y and determines whether or not the received operand represents a special operand. If not, the detector 24 or 26 simply outputs the operand x or y to the arithmetic section 14. However, if the detector 24 or 26 detects that the operand x or y represents a special operand, the detector 24 or 26 identifies the type of the operand -- the detector determines which of the special operands the received operand x or y represents. Col. 3, ll. 11-21.

7. FIG. 2 shows an exemplary special operand generator circuit 22 in greater detail. As shown, the special operand generator circuit 22 includes first and second multiplexers 222 and 224.

8. In the conventional circuit, the arithmetic section 14 outputs appropriate selector control signals to the multiplexer 222 to output a

resulting exponent, and to the multiplexer 224 to output a resulting magnitude of an arithmetic operation. Col. 3, ll. 42-45 and 60-63.

9. In the conventional circuit, when the result of an arithmetic operation is zero, the arithmetic section outputs selector control signals to the multiplexers 222 and 224 for selecting the eight '0' bits for the exponent and twenty-three '0' bits for the magnitude. Col. 3, ll. 66-67; col. 4, ll. 1-4.

10. FIG. 3 shows a conventional detector 24 or 26. As shown, the detector 24 or 26 includes two comparator circuits 252 and 254. Col. 4, ll. 24-26.

11. In the conventional circuit, three AND gates 261, 262, and 263 are also provided. The AND gate 261 receives as inputs the logic bits outputted on the lines 255 and 257. The AND gate 261 therefore outputs a signal indicating whether or not the operand represents a zero valued special operand. Col. 4, ll. 41-45.

PRINCIPLES OF LAW

Claim Interpretation

The *claims* measure the invention. *See SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). During prosecution before the USPTO, claims are to be given their broadest reasonable interpretation, and the scope of a claim cannot be narrowed by reading disclosed limitations into the claim. *See In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997); *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989); *In re Prater*, 415 F.2d 1393, 1404-05 (CCPA 1969).

Anticipation

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984).

ANALYSIS

Claim Interpretation

Claim 1 recites an analyzer circuit configured to determine a first status and a second status based on data within respective first and second floating point operands. Claim 1 further recites a results circuit coupled to the analyzer circuit and configured to "assert a resulting floating point operand containing the product of the first floating point operand and the second floating point operand and a resulting status embedded within the resulting floating point operand."

We interpret claim 1 as requiring at least: 1) a plurality of operands, each "containing" encoded status information, and 2) a results circuit that produces a resulting floating point operand containing both the product of the first and second floating point operands and status information.

The language of claim 1 does not preclude the product and the status information from being represented by the same data within the resulting floating point operand. *See* FF 4 for an example of a resulting floating point

operand whose bits result in a value of "zero" and whose bit string has been assigned a status of representing "zero."[2]

Section 102(b) Rejection

The Examiner finds that Huang describes the subject matter of instant claim 1 in the arrangement of Figure 4.[3] Ans. 4-5, 10-12. However, we agree with Appellant that Huang's "tag" and "floating-point value" are not disclosed as being part of the same "floating-point operand." *See* Ans. 11. Huang discloses, to the contrary, that the tag (status info) stands separate from the operand (result). FF 1, 2.

However, prior art Figures 1 through 3 of Huang discloses all the features of claim 1, including an analyzer circuit 24, 26 and a results circuit 14, 22. For the special case of a "zero" operand and another "zero" operand, the results circuit asserts a resulting floating point operand containing the product and a "resulting status" embedded into the resulting floating point operand as claimed.

Since Huang anticipates claim 1, we sustain the rejection. Claims 2-40, not separately argued, fall with claim 1. *See* 37 C.F.R. § 41.37(c)(1)(vii). However, because our decision relies on different reasoning from that of the Examiner's, we designate the decision as a new ground of rejection.

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[2] Claim 1 would distinguish over the cited prior art if the claim were amended to require a single resulting floating point operand that contains distinct parts which represent a value and encoded status information.

[3] For purposes of this appeal, claim 1 is representative of the other independent claims (15 and 28).

DECISION

The rejection of claims 1-40 under 35 U.S.C. § 102(b) as being anticipated by Huang is affirmed. We designate our decision as a new ground of rejection.

37 C.F.R. § 41.50(b) provides that "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that Appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .
>
> (2) *Request rehearing.* Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 41.50(f).

AFFIRMED -- 37 C.F.R. § 41.50(b)

msc

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